REMARKS/ARGUMENTS

Brief Summary of Status

Claims 30-58 are pending in the application.

Claims 35-42 are allowed.

Claims 30, 32-34, and 43-58 are rejected.

Claims 31 objected to.

In the above-referenced office action, the Examiner rejected claims 30, 32, and 33 under 35 U.S.C. §102(b) as being anticipated by Leung et al., A 3-V 45 mW CMOS Differential Bandpass Amplifier for GSM Receivers, 1998 IEEE (0-7803-4455-3/98) (hereinafter referred to as "Leung").

The Examiner also rejected claims 30, 32, and 33 under 35 U.S.C. §102(e) as being anticipated by Momtaz, et al. (U.S. Patent No. 6,864,558 B2) (hereinafter referred to as "Momtaz").

The Examiner rejected claims 34, 43-58 under 35 U.S.C. §103(a) as being unpatentable over Leung in view of Ryan, et al. (U.S. Patent No. 6,414,558 B1) (hereinafter referred to as "Ryan").

The Examiner rejected claim 34 under 35 U.S.C. §103(a) as being unpatentable over Momtaz in view of Ryan.

The Examiner has indicated that claim 31 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 35-42 are allowed.

35 U.S.C. §102(b) and 35 U.S.C. §102(e)

In the above-referenced office action, the Examiner rejected claims 30, 32, and 33 under 35 U.S.C. §102(b) as being anticipated by Leung.

The Examiner also rejected claims 30, 32, and 33 under 35 U.S.C. §102(e) as being anticipated by Momtaz.

The Applicant respectfully traverses.

In the above-referenced office action, the Examiner asserts:

"FIG. 5. of Leung et al. discloses an amplifier: comprising transistor Md can be read as current source; transistor M1+.can be read as a first differential transistor having a source, gate and drain, wherein the source of the first differential transistor is coupled to the current source; transistor M1- can be read as a second differential transistor having a source, gate and drain, wherein the source of the second differential transistor is coupled to the current source; resistor Ro connected to transistor M1+ can be read as a first output resistor having positive and negative ends, wherein the negative end of the first output resistor is coupled to the drain of the first differential transistor (M1+); resistor Ro connected to transistor M1- can be read as a second output resistor having positive and negative ends, wherein the negative end of the second output resistor is coupled to the drain of the second differential transistor (M1-); Inductor Lo connected to the first output resistor Ro connected to transistor M1+ can be read as a first shunt peaking inductor having positive and negative ends; wherein the negative end of the first shunt peaking inductor is coupled to the positive end of the first output resistor; and inductor Lo connected to the second output resistor Ro connected to transistor M1- can be read as a first shunt peaking inductor having positive and negative ends; wherein the negative end of the second shunt peaking inductor is coupled to the positive end of the first second resistor". (see office action, Part of Paper No./Mail Date 10, pp. 2-3).

The Examiner appears to assert that the connectivity of transistor M2+ (having its gate connected to the same voltage supply as the end of series resistor-inductor pair, Ro and Lo, the other end of which is connected to the drain of transistor M2+) is equivalent to that of the Applicant subject matter as claimed of being "coupled."

Also, the Examiner appears to assert that the connectivity of transistor M2- (having its gate connected to the same voltage supply as the end of series resistor-inductor pair, Ro and Lo, the other end of which is connected to the drain of transistor M2-) is equivalent to that of the Applicant subject matter as claimed of being "coupled."

The Applicant respectfully believes that the Examiner is not interpreting the Leung reference properly in this case. This is clearly not a mere "coupling" as is understood by those in the art. Rather, each of these connections of Leung (in FIG. 5) is through a corresponding n-channel CMOS transistor having a particular manner of configuration and connectivity as described above.

Moreover, the Applicant respectfully asserts that the Examiner also appears not to consider the series resistor-inductor pair, Rl and Ls, that couples the source of transistor M1+ to the current source (transistor Md) of Leung. Similarly, the Applicant respectfully asserts that the Examiner also appears not to consider the series resistor-inductor pair, Rl and Ls, that couples the source of transistor M1- to the current source (transistor Md) of Leung. The Examiner seems to assert that each of these resistor-inductor pairs, Rl and Ls, of the FIG. 5 of Leung are equivalent to the Applicant subject matter as claimed of being "coupled."

The Applicant respectfully believes that the Examiner is not interpreting the Leung reference properly in this case as well. This is clearly not a mere "coupling" as is understood by those in the art. Rather, each of these connections of Leung (in FIG. 5) is through a corresponding series resistor-inductor pair, Rl and Ls, having a particular manner of configuration and connectivity as described above.

To support a proper 35 U.S.C. §102(b) rejection, the cited reference must teach and disclose each and every element of the subject matter as claimed by the Applicant.

The Applicant respectfully believes that the inclusion of these additional components (i.e., resistor-inductor pairs, Rl and Ls, as well as the transistors, M2+ and M2-, and their unique connectivity and arrangement) is improper and does not lead the Applicant's claimed subject matter. Extending upon this analysis as apparently being performed by the Examiner, it appears that the Examiner would perhaps deem it appropriate to include an even wider variety of components besides a "first output impedance" connected to the "drain of the first differential transistor" and a "second output impedance" connected to the "drain of the second differential transistor" as claimed by the Applicant in claim 31. The Applicant respectfully traverses this analysis as being made by the Examiner.

The Applicant has amended independent claim 30 and its dependent claims 31 and 34.

The Applicant respectfully asserts that each of Leung or Momtaz fails to teach or disclose the subject matter as claimed by the Applicant in claim 30 that includes an amplifier stage, comprising: a current source; a first differential transistor having a source, gate, and drain, wherein the source of the first differential transistor is coupled to

the current source; a second differential transistor having a source, gate, and drain, wherein the source of the second differential transistor is coupled to the current source; a first miller capacitance cancellation capacitor having positive and negative ends, wherein the positive end of the first miller capacitance cancellation capacitor is coupled to the drain of the second differential transistor, and wherein the negative end of the first miller capacitance cancellation capacitor is coupled to the gate of the first differential transistor; and a second miller capacitance cancellation capacitor having positive and negative ends, wherein the positive end of the second miller capacitance cancellation capacitor is coupled to the drain of the first differential transistor, and wherein the negative end of the second miller capacitance cancellation capacitor is coupled to the gate of the second differential transistor.

The Applicant respectfully believes that claim 30 is allowable. The Applicant respectfully believes that claims 32 and 33, being further limitations on the subject matter of claim 30, are also allowable. The Applicant respectfully requests that the Examiner withdraw the rejection of claims 30, 32, and 33 under 35 U.S.C. §102(b) as being anticipated by Leung, and the Applicant respectfully requests that the Examiner withdraw the rejection of claims 30, 32, and 33 under 35 U.S.C. §102(e) as being anticipated by Momtaz.

35 U.S.C. §103(a)

The Examiner rejected claims 34, 43-58 under 35 U.S.C. §103(a) as being unpatentable over Leung in view of Ryan.

The Applicant respectfully asserts that the combination of Leung and Ryan (and the inclusion of Ryan in combination with Leung) fails to teach or disclose the subject matter as claimed by the Applicant in claim 30 that includes an amplifier stage, comprising: a current source; a first differential transistor having a source, gate, and drain, wherein the source of the first differential transistor is coupled to the current source; a second differential transistor having a source, gate, and drain, wherein the source of the second differential transistor is coupled to the current source; a first miller capacitance cancellation capacitor having positive and negative ends, wherein the positive end of the first miller capacitance cancellation capacitor is coupled to the drain of the second differential transistor, and wherein the negative end of the first miller

capacitance cancellation capacitor is coupled to the gate of the first differential transistor; and a second miller capacitance cancellation capacitor having positive and negative ends, wherein the positive end of the second miller capacitance cancellation capacitor is coupled to the drain of the first differential transistor, and wherein the negative end of the second miller capacitance cancellation capacitor is coupled to the gate of the second differential transistor.

The Applicant respectfully believes that claim 34, being a further limitation on the subject matter of claim 30, is also allowable.

As such, the Applicant respectfully requests that the Examiner withdraw the rejection of claim 34 under 35 U.S.C. §103(a) as being unpatentable over Leung in view of Ryan.

With respect to claims 43-58, in the above-referenced office action, the Examiner asserts:

"Regarding claims 43-58, although Leung et al. does not have multistage differential amplifier, Ryan et al. teaches in FIG. 3A a multistage differential amplifier, therefore it would have been obvious at the time the invention was made to a person having ordinary skill in the at to use the differential amplifier of Leung et. al. in the circuit of Ryan et al. in order to have an optimum performance for the circuit." (see office action, Part of Paper No./Mail Date 10, p. 5).

With respect to claims 43-58, the Applicant respectfully asserts that the Examiner fails properly to deal with at least the limitations of "first pair of miller capacitance cancellation capacitors" (in at least Applicant's claim 43) and "first pair of miller capacitance cancellation capacitors" and "second pair of miller capacitance cancellation capacitors" (in at least Applicant's claim 54).

The Applicant respectfully points out that the Ryan reference contains no reference whatsoever to "miller" type capacitance cancellation capacitors or miller capacitors.

Ryan does refer to some capacitors, C1, C2, C3, C4, C5, and C6, but each of these is described as being "decoupling capacitors" that "remove DC offset associated with the preceding amplification stage". (e.g., see Ryan, col. 5, lines 60-64). There is no

reference of any "miller" type capacitance cancellation capacitors or miller capacitors in Ryan.

The Leung reference does in fact disclose some reference to "Miller capacitor" as provide below, but in a different manner as within the Applicant's claimed subject matter.

"A Miller capacitor is used to adjust the center frequency of the amplifier by varying the gain of the Miller amplifier and thus equivalent capacitance at the output node. With the center frequency tuning circuit, the effective Q id degraded due to the introduction of the Miller capacitor Cm and the output resistance Rm of the Miller amplifier." (see Leung, top of left hand column, p. IV-343).

The Applicant respectfully points out that this "Miller capacitor" and "Miller amplifier" of Leung is located in a portion/stage of FIG. 5 of Leung not even referred to by the Examiner when referencing Leung.

In contradistinction, the Examiner refers to "transistor M1+", "transistor M1-", "resistor Ro", and "inductor Lo", which are located in an entirely different stage of FIG. 5 of Leung than the "Miller capacitor" and "Miller amplifier" of Leung that the Applicant identifies above.

Moreover, the "Miller capacitors", "Cm-" and "Cm+", of Leung are connected between the drain and gate of each of the "transistor Mf+" and "transistor Mf-", respectively. More specifically within FIG. 5 of Leung, a first "Miller capacitor", "Cm-", is connected between the drain and gate of the single "transistor Mf+". Similarly, within FIG. 5 of Leung, a second "Miller capacitor", "Cm+", is connected between the drain and gate of the single "transistor Mf-". Each of the "Miller capacitors", "Cm-" and "Cm+", of Leung is connected to only one single transistor, namely, "transistor Mf+" or "transistor Mf-". There is no connectivity of the "Miller capacitors", "Cm-" and "Cm+", in any way, to more than one transistor within the "Miller amplifier" depicted in FIG. 5 of Leung.

The Applicant again respectfully points out that the Applicant's claimed subject matter of claim 43 and claim 54 did in fact include the limitations of "first pair of miller capacitance cancellation capacitors" (Applicant's claim 43) and "first pair of miller capacitance cancellation capacitors" and "second pair of miller capacitance cancellation

capacitors" (Applicant's claim 54) in a previous filing of the present U.S. utility patent application.

However, in an effort to expedite prosecution and for clarification, the Applicant has amended the claims 43 and 54 to show more clearly the connectivity of at least one miller capacitance cancellation capacitor contained within the Applicant's claimed subject matter in each of the claims 43 and 54.

In light of the Examiner' statements of reasons for the indication of allowable subject matter within the above referenced office action (see office action, Part of Paper No./Mail Date 10, p. 6), the Applicant respectfully believes that the claim 43-58 are allowable.

Specifically, the Applicant respectfully believes that claims 43 and 54 are allowable, and that claims 44-53, being further limitations on the subject matter of claim 43, are also allowable, and that claims 55-58, being further limitations on the subject matter of claim 54, are also allowable.

As such, the Applicant respectfully requests that the Examiner withdraw the rejection of claim 43-58 under 35 U.S.C. §103(a) as being unpatentable over Leung in view of Ryan.

The Examiner also rejected claim 34 under 35 U.S.C. §103(a) as being unpatentable over Momtaz in view of Ryan.

The Applicant respectfully points out that the Momtaz reference contains no reference whatsoever to "miller" type capacitance cancellation capacitors or miller capacitors. The only time the word "Miller" even appears in Momtaz is with respect to the listing of U.S. patent documents cited on page 2 of Momtaz, namely "5,406,615 A 4/1995 Miller, II et al.". The Applicant also respectfully points out that the only reference of the word "Miller" in the "5,406,615 A 4/1995 Miller, II et al." reference is pertaining to the first inventor's name; there is no mention of "miller" type capacitance cancellation capacitors or miller capacitors therein.

The Applicant again respectfully points out that the Ryan reference contains no reference whatsoever to "miller" type capacitance cancellation capacitors or miller capacitors.

The Applicant respectfully asserts that the combination of Momtaz and Ryan fails to teach or disclose the subject matter as claimed by the Applicant in claim 30 that includes an amplifier stage, comprising: a current source; a first differential transistor having a source, gate, and drain, wherein the source of the first differential transistor is coupled to the current source; a second differential transistor having a source, gate, and drain, wherein the source of the second differential transistor is coupled to the current source; a first miller capacitance cancellation capacitor having positive and negative ends, wherein the positive end of the first miller capacitance cancellation capacitor is coupled to the drain of the second differential transistor, and wherein the negative end of the first miller capacitance cancellation capacitor is coupled to the gate of the first differential transistor; and a second miller capacitance cancellation capacitor having positive and negative ends, wherein the positive end of the second miller capacitance cancellation capacitor is coupled to the drain of the first differential transistor, and wherein the negative end of the second miller capacitance cancellation capacitor is coupled to the gate of the second differential transistor.

The Applicant respectfully believes that claim 34, being a further limitation on the subject matter of claim 30, is also allowable.

Applicant respectfully requests that the Examiner withdraw the rejection of claim 34 under 35 U.S.C. §103(a) as being unpatentable over Momtaz in view of Ryan.

Allowable Subject Matter

The Examiner has indicated that claim 31 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 35-42 are allowed.

The Applicant has amended claim 30, and the Applicant respectfully believes that claim 30 is allowable. Moreover, the Applicant respectfully believes that claim 31, being a further limitation on the subject matter of claim 30, is also allowable.

The Applicant respectfully believes that claims 30-58 are in condition for allowance and respectfully requests that they be passed to allowance.

The Examiner is invited to contact the undersigned by telephone or facsimile if the Examiner believes that such a communication would advance the prosecution of the present patent application.

RESPECTFULLY SUBMITTED,

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